VI-4 ITERATIVE SYNTHESIS OF VARACTOR-MULTIPLIER MICROWAVE NETWORKS AND A DOUBLER WITH 0.17 WATT OUTPUT AT 47 GHz

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The use of dynamic impedance contours in the design and evaluation of microwave varactor circuits has been described by Kurokawa.[1] His work was directed primarily toward parametric amplifiers. Kurokawa developed lossless circuit models to represent input and pump coupling networks for varactor diodes in microwave circuits. C. B. Swan[2] used similar methods in the evaluation of a microwave varactor tripler. Swan included one component of circuit loss in his model and explained the characteristics of optimum dynamic impedance contours* for a tripler. We present optimum contours for the input and output networks of all varactor multipliers and a simple calculation of overall circuit efficiency in the presence of lossy coupling networks. We also present the results for a varactor doubler designed for 23.5-47 GHz with an output power of 173 mW and an efficiency of 33%.

Consider a varactor diode embedded in a linear bilateral network from which two transmission lines extend to from the input and output ports of a varactor multiplier circuit, as shown in Fig. 1a. Through proper choice of the input and output reference planes the circuit model takes the form illustrated in Fig. 1-b. The generality of this representation is not limited by the presence of the ideal transformers and filters. The shunt loss elements R_{p1} and R_{p2} are indicative of circuit losses and poor isolation between input and output circuits. Their values are directly related to the values of the dissipation factors D_1 and D_2 in the ideal dynamic impedance contour of Fig. 2. The series loss elements R_{s1} and R_{s2} include the varactor series resistance, as well as contact resistance and other losses that reduce the dynamic Q of the input and output circuits. Input and output "dynamic Q's" are defined by Eqs. 8 and 9 in Fig. 3. The series inductive elements L_1 and L_2 resonate the elastance of the varactor junction at the bias point corresponding to the tuning points T_1 and T_2 in Fig. 2. Under conditions of optimum tuning, the relationships between the series inductance and the series resistances are $(\omega L_1/R_{s1}) = \hat{S}_1 Q'$ and $(2\omega L_2/R_{s2}) =$ (the values of $\hat{S}_1$ and $\hat{S}_n$ have been published.[3, 4, 5])

A set of optimum contours for the input and output networks of a varactor doubler are shown in Fig. 2. The points have been calculated for a nominally driven abrupt junction doubler. Values for the tuning points T_1 and T_2 were calculated from Eqs. 4 and 5 in Fig. 3. It should be noted that these contours are independent of the impedance level to which they are normalized, as long as the load impedance under operating conditions has the same value. In this example, Q' is less than 2Q'' so that Eq. 6 in Fig. 3 is applicable for determining the overall circuit efficiency.

Optimum dynamic impedance contours are independent of specific values of junction capacitance, so that all information about power-handling capability or the power required to achieve optimum performance is missing. In other words, the same contours apply independently of the power levels involved in the actual circuit. In summary, there is a single optimum set of dynamic impedance contours for the input and output circuits of a multiplier of order N that incorporates a varactor of a particular type, such as an abrupt or graded junction, and the characteristics of this set of optimum contours are given by the equations in Fig. 3.

Figures 4 and 5 relate to the doubler discussed in the experimental section. Measured data are shown in Fig. 5, while the dynamic impedance contours of Fig. 4 were computed by using the circuit model and element values given in Fig. 1.

EXPERIMENTAL RESULTS

The design of the 23.5-47 GHz doubler was accomplished in the following way: We constructed a diode test fixture at 47 GHz consisting of a step transformer, a low-impedance waveguide section in which the diode was mounted, and fixed back short. This fixture served as a model for the doubler output circuit. Diodes were placed in the fixture, and dynamic impedance contours were evaluated. The design was modified as indicated by the measurements until a nearly optimum dynamic impedance contour was effected.

Twenty-nine Sylvania D5147E Series GaAs varactor were measured in the finished model of the output circuit. Because of the extremely compact design and careful attention to minimization of reactive energy storage, all 29 diodes were found to be resonant for some value of reverse bias between −2 and −7 volts, even though the zero bias capacitance range was greater than a factor 2. The Q'' value for 22 diodes was greater than 10. The highest value measured was 27, which indicated a dynamic cutoff frequency greater than 1200 GHz. If the measured "D" value for a given diode was less than 20, the test fixture was disassembled, cleaned, refinished, and reassembled, and the test was repeated. In all cases except one, the fixture, not the diode, was held responsible for the measured losses.

The first attempt to construct a doubler incorporating the completed output circuit was unsuccessful. Low values for D_2 indicated poor isolation between the input and output ports. After this was corrected, by installing a three section filter, dynamic impedance contours obtained from the doubler output circuit were virtually identical with those obtained in the test fixture.

As can be seen in Fig. 5, the input circuit contour for diode #27 is not optimum. About two or three more modifications will be necessary to make it so. We have tested four diodes in the doubler model of Fig. 1: Diode #8 gave 111 mW output with 30% efficiency, #29 gave 60 mW output with 38% efficiency, and #18 gave 173 mW output with 33% efficiency. Results for diode #27 are presented in Fig. 6. In all cases, the efficiency calculated from Eq. 6 was within 0.5 db of the measured value. The VSWR for diode #27, calculated from Eq. 10, was 1.85:1, compared with a measured value of 2.5:1. The discrepancy is a result of improper reactive tuning in the input network. All measurements of power at 47 GHz were made with a PRD Model 666 dry-load calorimeter. Input power measurements were made with a Hewlett-Packard 431-B power meter that had been calibrated against the PRD calorimeter.

The method that we have described permits the microwave engineer to carry through a multiplier design with his feet firmly on the ground, predict the outcome in advance of completion, and be able to quantitatively and qualitatively evaluate each modification and its expected results. Finally, the maximum power output level of 173 mW is, at present, limited by the available power at 23.5 GHz.

Although our goal is 50 mW output at 50% efficiency, we are confident that a quarter of a watt output is easily attainable.

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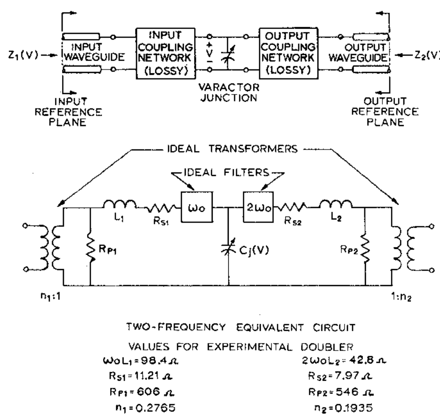

FIG. 1 - Circuit Model

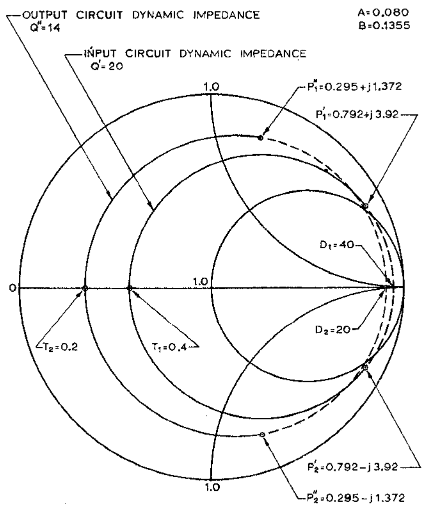

FIG. 2 - Ideal Dynamic Impedances

IF, FOR AN OPTIMUM MULTIPLIER,

$$R_{LOAD} = B\frac{S_{max}}{\omega_o} \qquad (1)$$

$$R_{IN} = A\frac{S_{max}}{\omega_o} \qquad (2)$$

AND

$$\text{EFFICIENCY} = e^{-\alpha\frac{\omega_{out}}{\omega_c}} \qquad (3)$$

WHERE

ω_o = INPUT FREQUENCY

AND ω_c = CUTOFF FREQUENCY

THEN, FOR AN OPTIMALLY TUNED CIRCUIT,

$$T_1 = \frac{1}{1+\frac{D_1-1}{D_1}AQ'} \qquad (4)$$

$$T_2 = \frac{1}{1+(1+D_2)(1+2BQ'')} \qquad (5)$$

AND

$$\text{EFFICIENCY} = \begin{cases} \dfrac{D_2(D_1-1)\,e^{-\frac{\alpha}{Q''}}}{D_1(1+D_2)\left(1+\frac{1}{AQ'}-\frac{1}{2AQ''}\right)} & \text{FOR } Q' \leqslant 2Q'' \qquad (6) \\[2ex] \dfrac{D_2(D_1-1)\,e^{-\frac{2\alpha}{Q'}}}{D_1(1+D_2)\left[1+\frac{(D_2^2+1)(Q'-2Q'')}{(2BQ'Q''+2Q''-Q')}\right]} & \text{FOR } Q' \geqslant 2Q'' \qquad (7) \end{cases}$$

WHERE Q' AND Q'' MAY BE FOUND AS FOLLOWS: LET $P = r + jX$ AND $q = \frac{|X|}{r}$ PROPERLY SCRIPTED FOR EACH OF THE FOUR POINTS LABLED "P" IN FIGURE 2. THEN

$$Q' = \frac{q_1'}{1-\frac{r_1'}{D_1}\left[1+(q_1')^2\right]} + \frac{q_2'}{1-\frac{r_2'}{D_1}\left[1+(q_1')^2\right]} \qquad (8)$$

$$Q'' = \frac{q_1''}{1+\frac{r_1''}{D_2}\left[1+(q_1'')^2\right]} + \frac{q_2''}{1-\frac{r_2''}{D_2}\left[1+(q_2'')^2\right]} \qquad (9)$$

IF THE OUTPUT CIRCUIT COUPLING IS CORRECT, THEN THE INPUT VSWR UNDER DRIVE CONDITIONS MAY BE COMPUTED FROM

$$\text{VSWR} = \frac{T_1\,D_1(1+AQ')}{D_1+T_1AQ} \qquad (10)$$

FIG. 3 - Equations

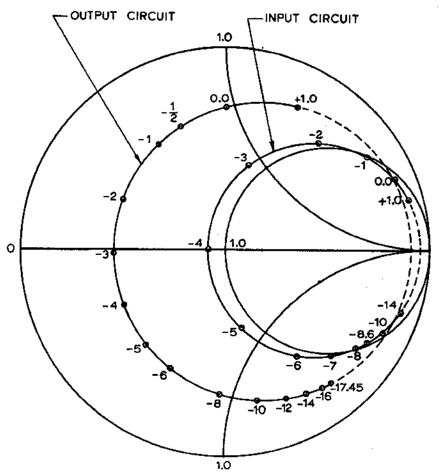

FIG. 4 - Calculated Dynamic Impedances

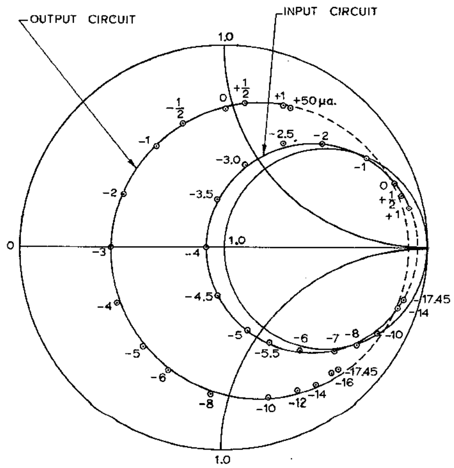

FIG. 5 - Measured Dynamic Impedances

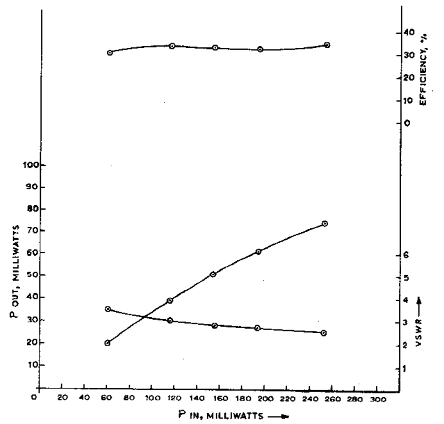

FIG. 6 - Experimental Doubler Results